REMARKS/ARGUMENTS

Claims 1-3 and 5-7 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Higashi*** (US 6,023,260).

Allowable Subject Matter

Claims 4 and 8 are identified as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Amendments to the Claims

Claims 1, 3, 5, and 7 are cancelled without prejudice.

Claim 2 is amended to independent form by including the limitations of claim 1 and a limitation that the value of the capacitor is determined according to the feed-through voltage drop.

Claim 4 is amended to independent form by including the limitations of claims 1 and 3 and thus should now be in condition for allowance.

Claim 6 is amended to independent form by including the limitations of claim 5 and a limitation that the value of the capacitor is determined according to the feed-through voltage drop.

Claim 8 is amended to to independent form by including the limitations of claims 5 and 7 and thus should now be in condition for allowance.

Claims 2, 4, 6, and 8 are presently pending.

Claim Rejections

Claim 2:

Claim 2 is amended to independent form by including the limitations of claim 1 and a limitation that the value of the capacitor is related to the feed-through voltage drop.

Original claim 2 was rejected under 35 U.S.C. 102(b) as being anticipated by ***Higashi***. Applicant respectfully traverses the 35 U.S.C. 102(b) rejection for at least the following reason.

Higashi **does not teach, disclose or suggest a capacitor whose value determines a feed-through voltage drop of the first TFT.**

According to Fig. 3 and lines 29-30, column 6 of ***Higashi***, the reference number 412 is the capacitance of the data line itself (called data line capacitance). The data line capacitance 412 is formed between a drain/source of the MOS transistor 410 and a common voltage. A person skilled in the art knows that each signal line has an equivalent capacitance, such as the data line capacitance 412. The value of the data line capacitance 412 is determined according to the characteristic of the data line, such as its length and/or width of the data line. The value of the data line capacitance 412 can not be easily changed for counteracting the feed-through voltage drop caused by a parasitic capacitor of the MOS transistor 410.

According to line 18, page 8 to line 2, page 9 of the present application, a formula of the feed-through voltage drop ΔV is presented, wherein the equivalent capacitance of the data electrode (C_{DL}) and the storage capacitance of the display unit (C_{PIX}) are constants, and the capacitance of the counteracting device (C_{add}) is changed for reducing the of feed-through voltage drop ΔV. In other words, the feed-through voltage drop ΔV changed as a function of the capacitance of the counteracting device (C_{add}).

In the amended claim 2 of the present application, a sampling circuit comprises a first TFT and a capacitor. The capacitor is coupled between the second electrode and a reference potential node. The feed-through voltage drop caused by a parasitic capacitor between the second electrode and the control electrode of the first TFT is determined according to the value of the capacitor.

When the clock signal is changed from the first logic level to a second logic level, the capacitor reduces the feed-through voltage drop. The value of such a capacitor related to the feed-through voltage drop is not disclosed in ***Higashi***.

For these reasons alone, the amended claim 2 is patentable over ***Higashi***.

Claim 6:

Claim 6 is amended to an independent claim by all of the limitations of claim 5 and the limitations of that the value of the capacitor is related to the feed-through voltage drop.

Original claim 6 was rejected under 35 U.S.C. 102(b) as being anticipated by ***Higashi***. Applicant respectfully traverses the 35 U.S.C. 102(b) rejections for at least the following reason.

Higashi **does not teach, disclose or suggest a capacitor whose value determines a feed-through voltage drop of the first TFT.**

According to Fig. 3 and lines 29-30, column 6 of ***Higashi***, the reference number 412 is the capacitance of the data line itself (called data line capacitance). The data line capacitance 412 is formed between a drain/source of the MOS transistor 410 and a common voltage. A person skilled in the art knows that each data line has an equivalent capacitance (that is the data line capacitance 412). The value of the data line capacitance 412 is determined according to the characteristic of the data line, such as the length and/or width of the data line. The value of the data line capacitance 412 can not be readily changed for counteracting the feed-through voltage drop caused by a parasitic capacitor of the MOS transistor 410 since it is governed by how the device is laid out.

According to line 18, page 8 to line 2, page 9 of the present application, a formula for the feed-through voltage drop ΔV is presented, wherein the

equivalent capacitance of the data electrode (C_{DL}) and the storage capacitance of the display unit (C_{PIX}) are constants, and the capacitance of the counteracting device (C_{add}) is changed for reducing the of feed-through voltage drop ΔV. In other words, the feed-through voltage drop ΔV changed as the capacitance of the counteracting device (C_{add}).

In the amended claim 6 of the present application, a sampling circuit comprises a first TFT and a capacitor. The capacitor is coupled between the second electrode and a reference potential node. The feed-through voltage drop caused by a parasitic capacitor between the second electrode and the control electrode of the first TFT is determined according to the value of the capacitor. When the clock signal is changed from the first logic level to a second logic level, the capacitor reduces the feed-through voltage drop. The value of such a capacitor related to the feed-through voltage drop is not disclosed in ***Higashi***.

For these reasons alone, the amended claim 6 is patentable over ***Higashi***.

Conclusion

For the reasons noted above, applicant believes that claims 2, 4, 6, and 8 are allowable in their present amended form. Withdrawal of the rejections and allowance of the claims are respectfully requested.

Should the Examiner feel that further discussion of the application and the amendment might be conductive to closing prosecution and allowance thereof, please do not hesitate to contact the undersigned.

Withdrawal of the rejections and allowance of the claims are respectfully requested.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Office with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

June 14, 2007
(Date of Transmission)

Mary Ngo
(Name of Person Transmitting)

(Signature)

June 14, 2007
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Respectfully submitted,

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